

# The Allen Telescope Array

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UC Berkeley

## **Collaboration**

### *UC Berkeley Radio Lab*

Welch, Backer, Heiles, Blitz, Bower, Dexter, Urry,  
Engargiola, Fleming, Kraybill, Lugten, Wright

### *SETI Institute*

Tarter, Davis, Drake, Dreher, Ackerman, Deboer,  
Harp

### *CASPER/BWRC*

Werthimer, Cheng, Nagpal, Wawrzynek, Parsons

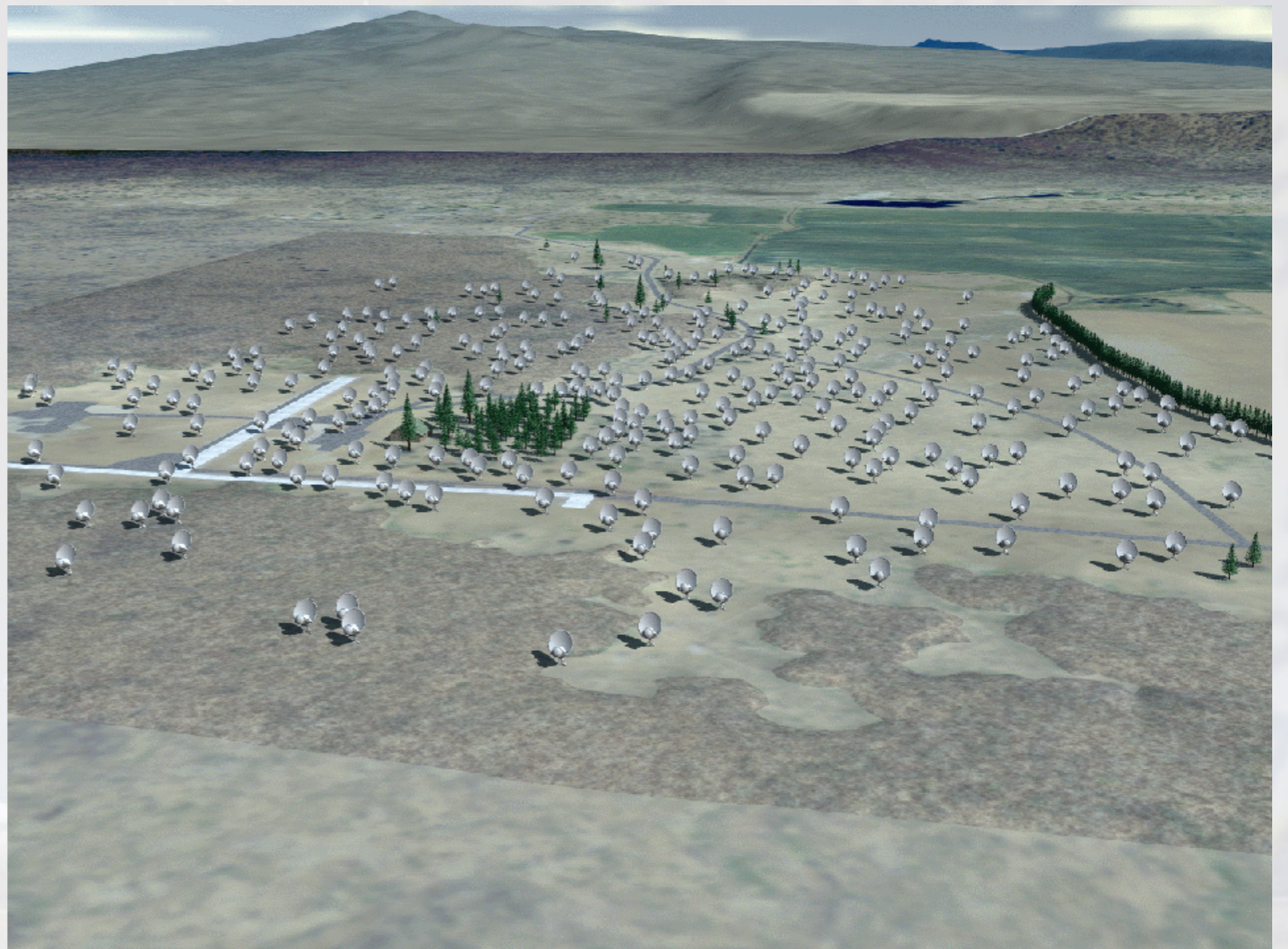


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## Telescope concept

A survey telescope — exploit decreasing back-end electronics and satellite-dish costs.

*cf. Seti 2020 (1997)*



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## Telescope design – Dish

Dishes are 6.1m primary/2.4m secondary offset Gregorian, for a 2.5 degree FoV.



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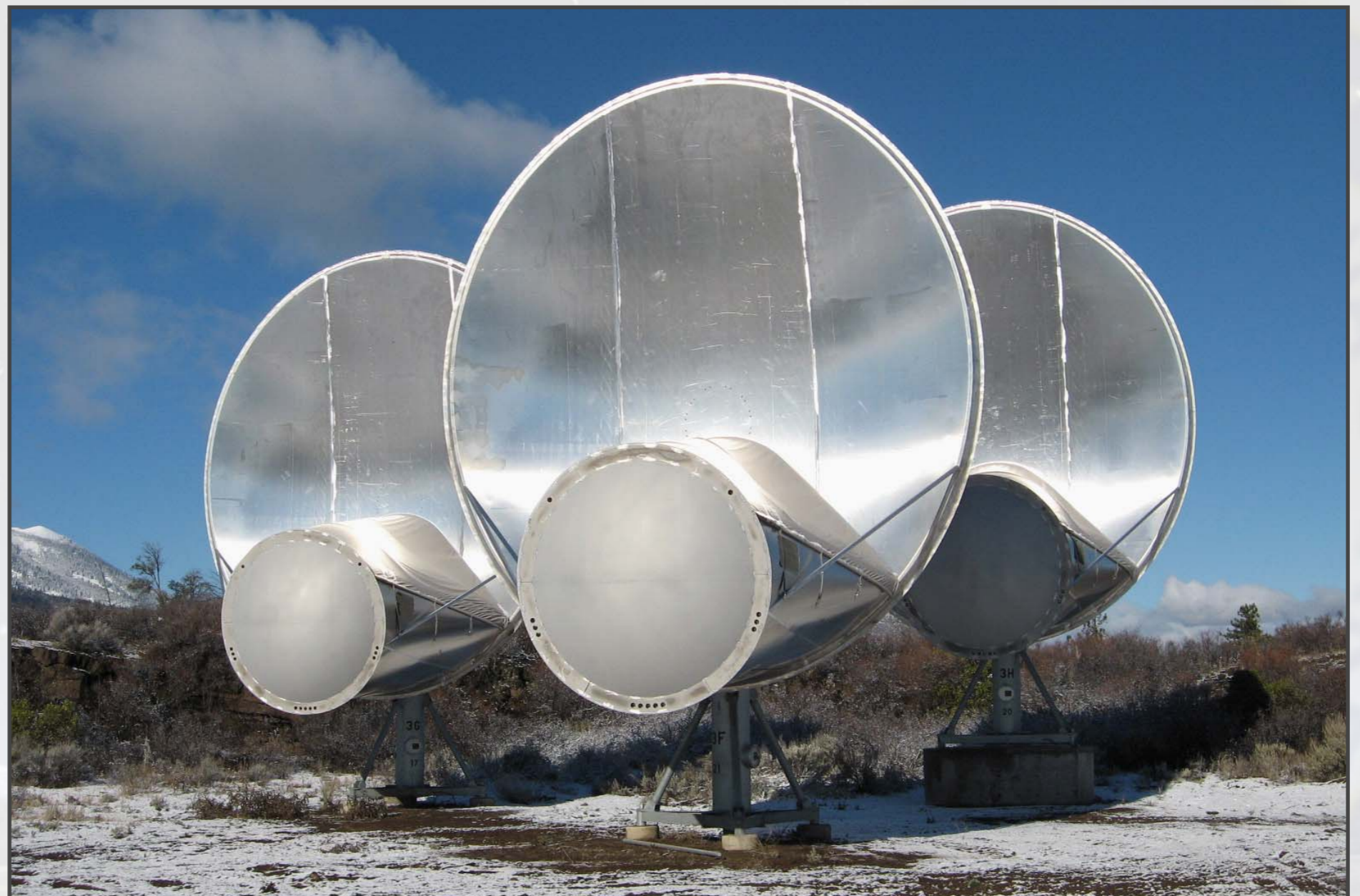
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## Telescope design — Feed

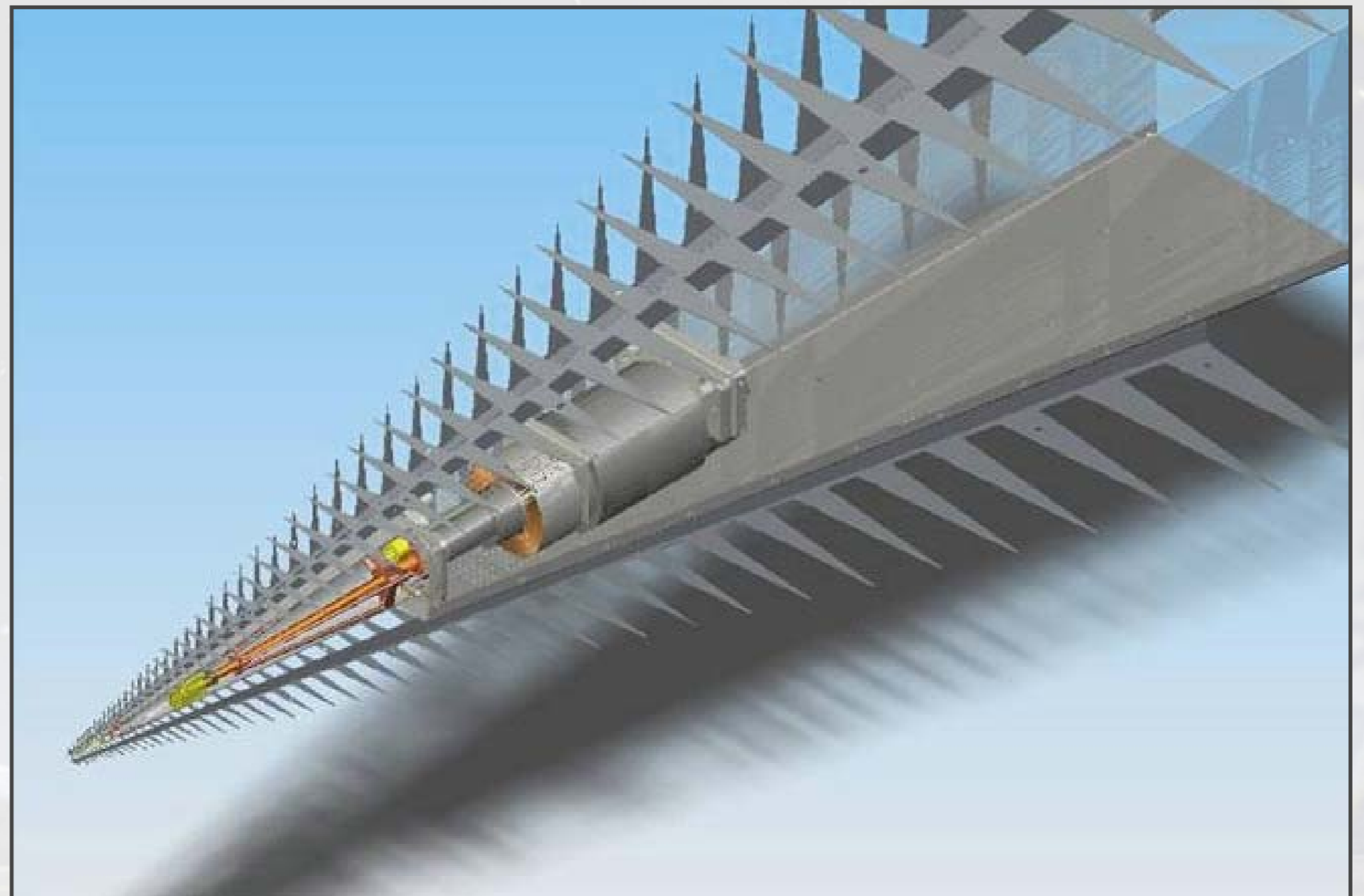
Log-periodic feed, for 4 octaves 0.5–11 GHz



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## Telescope design – Feed

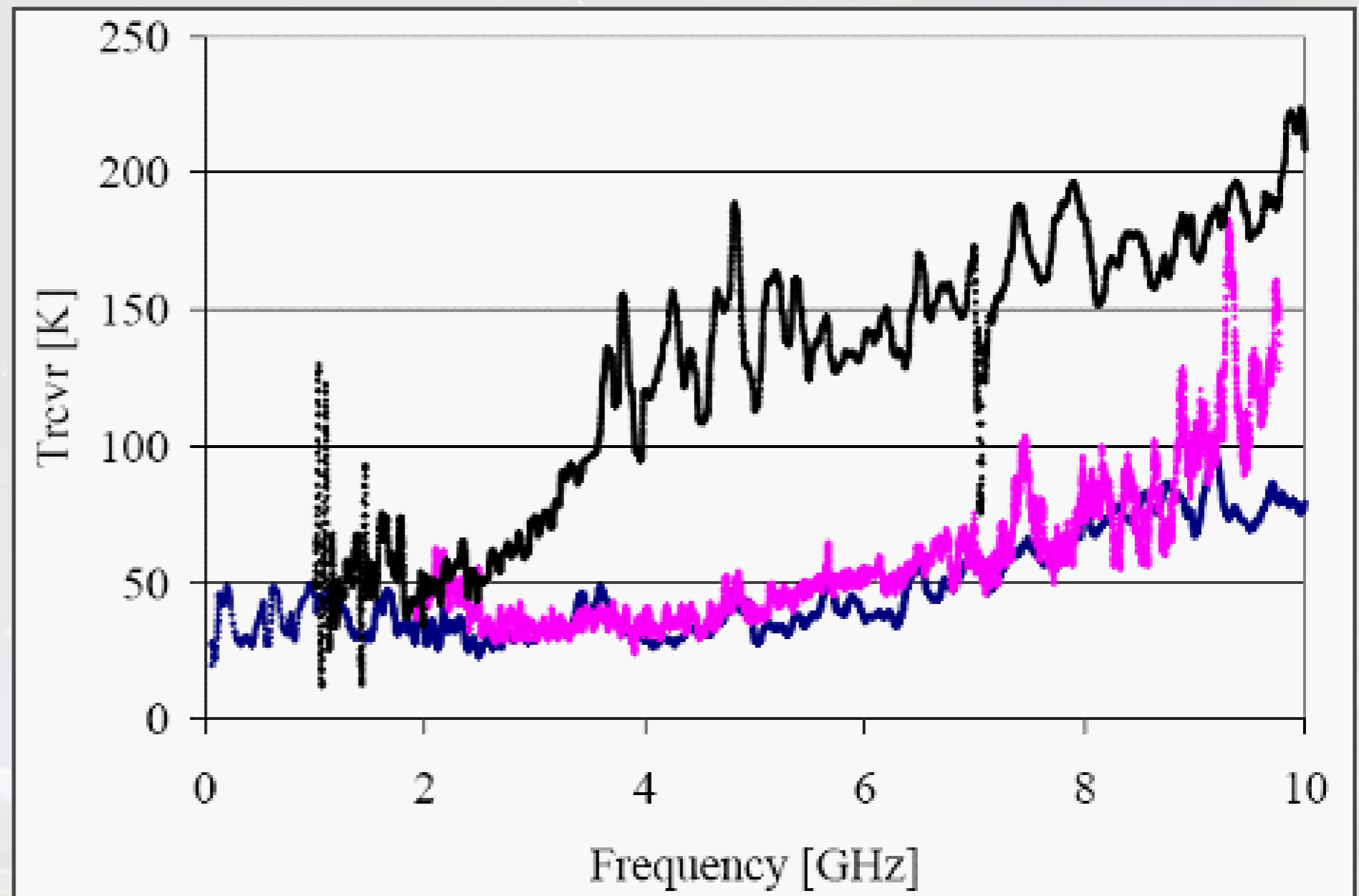
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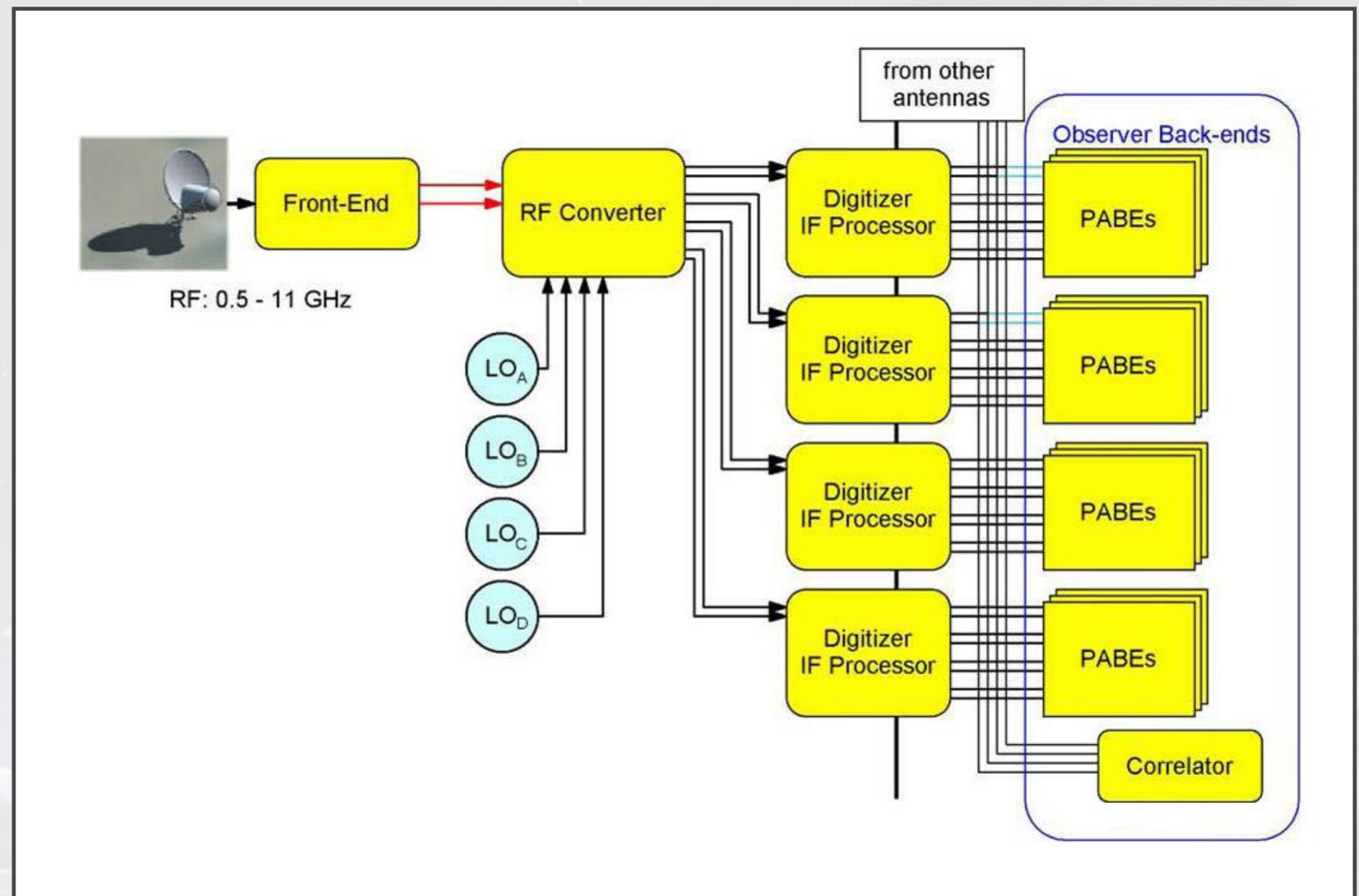
## Telescope design — Feed

Log-periodic feed, for 4 octaves 0.5–11 GHz



## Telescope design – IFs

4 Tunable IFs anywhere in the band



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## Beamformer

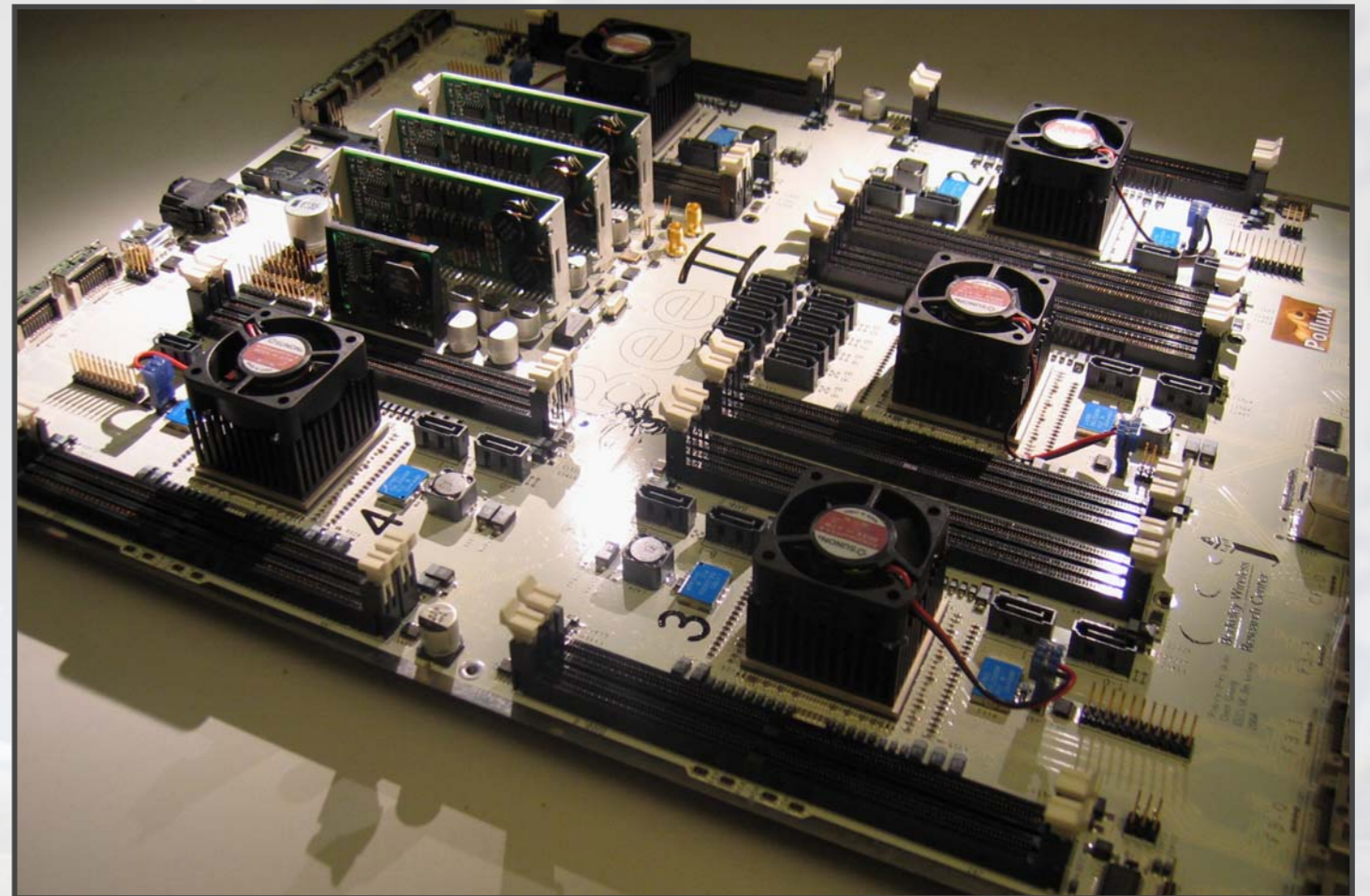
*CASPER*: Low cost, rapid development

Open-source, collaborative

Reusable, platform-independent gateway

Modular, scalable, upgradeable hardware

Industry standard communication protocols





# Beamformer

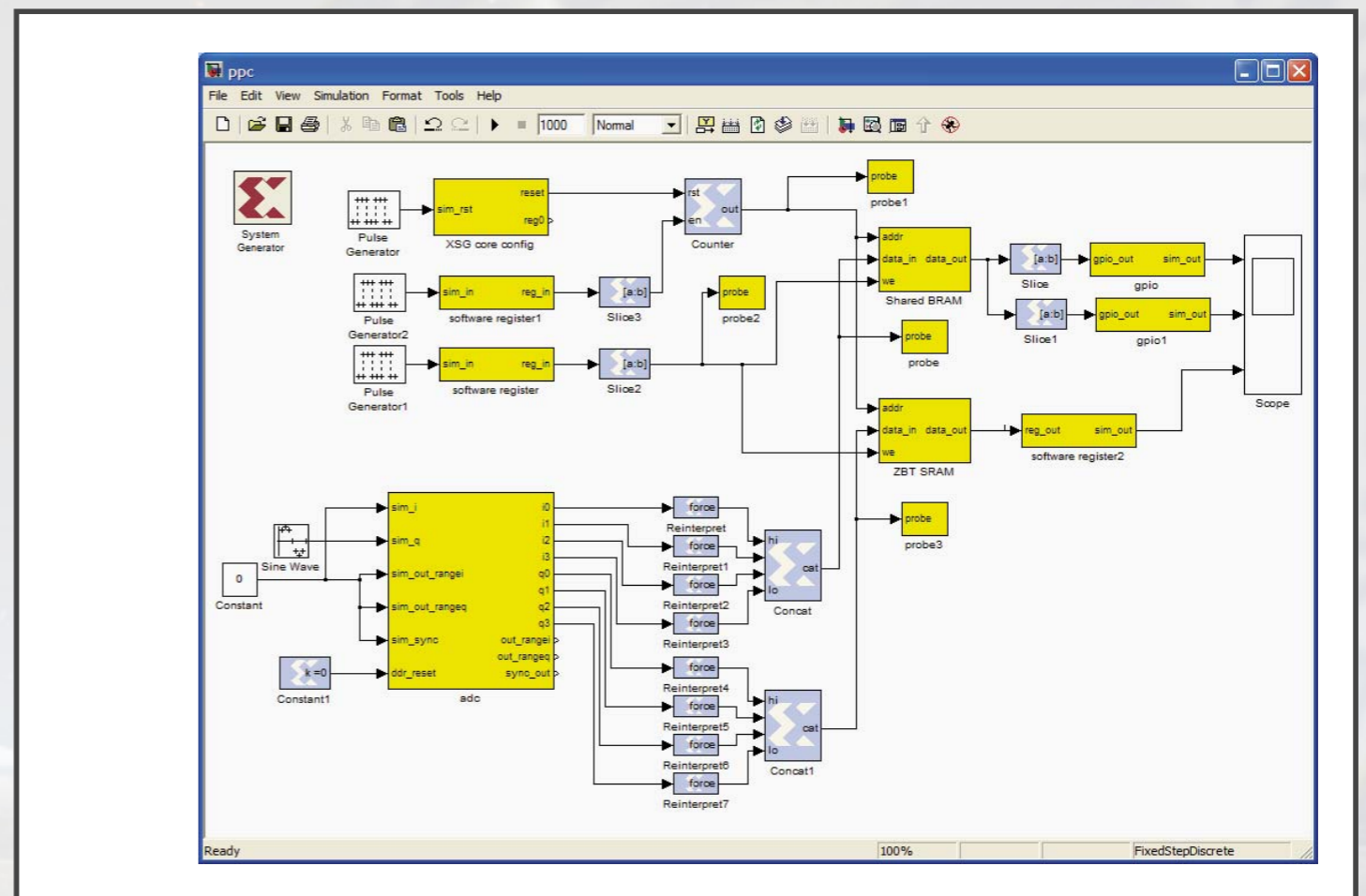
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## **Pulsar processor**

Scalable, upgradable:

Multi-IF FPGA based digital filterbank

Multi-IF FPGA/CPU coherent dedisperser



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## Status

Largely privately funded construction

Operational by July 1, 2007:

- 42-antenna array

- 42-element 3-beam 200MHz-BW beamformer

- 32-element correlator



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## First Science

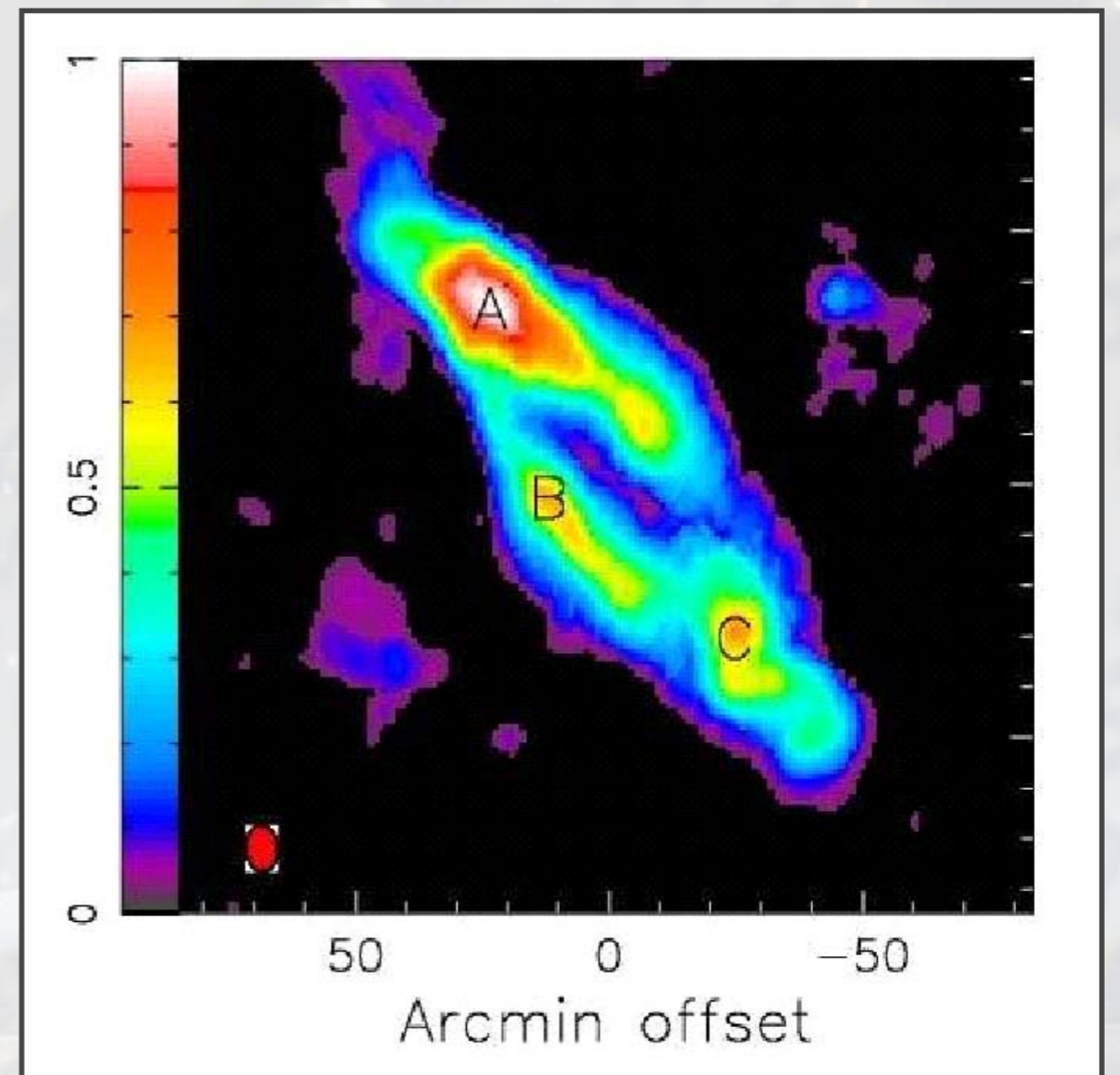
After July 1st, 2007

First SETI survey, 3 beams, 100MHz BW

FiGGS: 5GHz Sky Survey

First pulsar/ISM work

*M31 ATA-3*



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## First Science

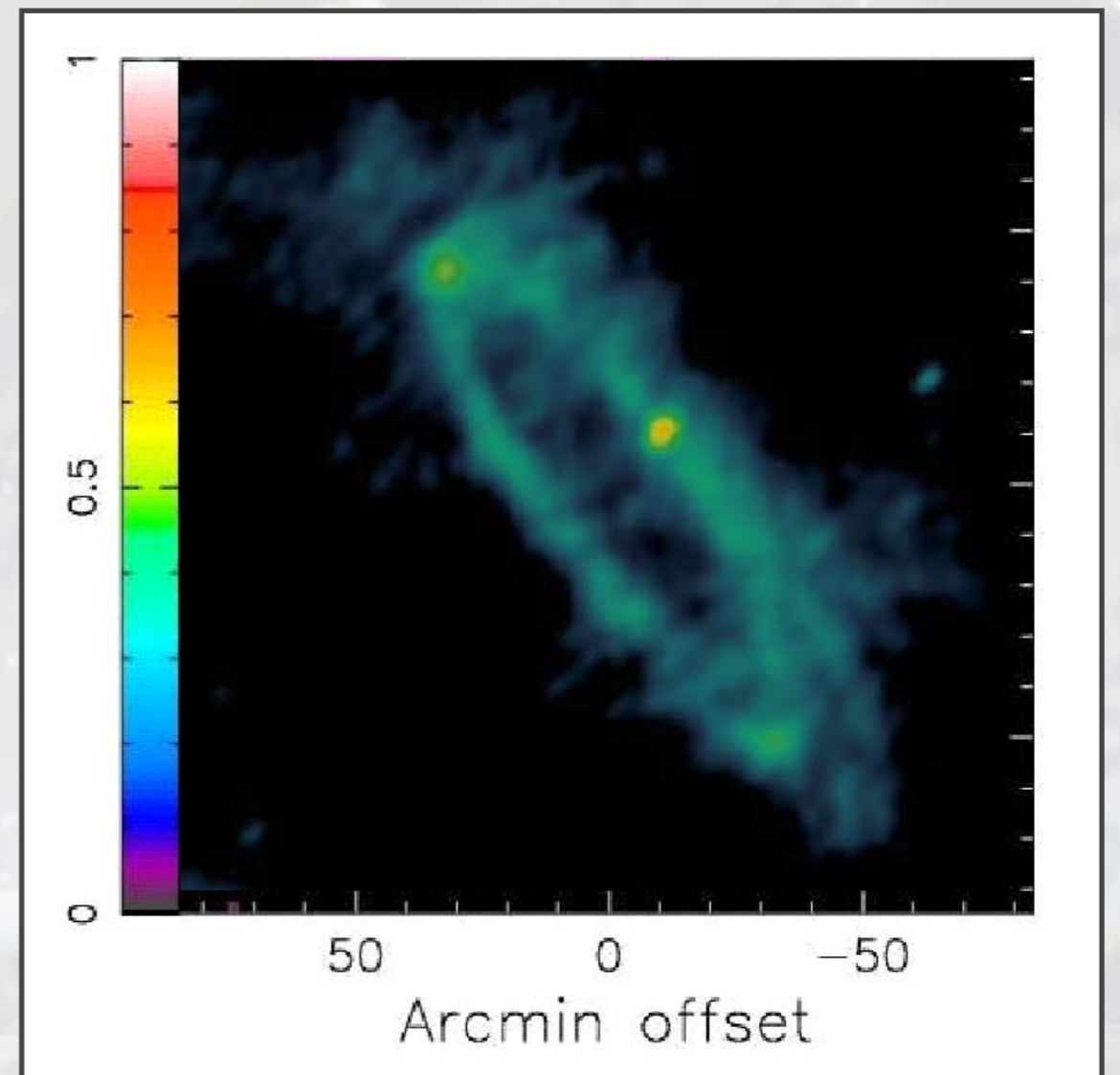
After July 1st, 2007

First SETI survey, 3 beams, 100MHz BW

FiGGS: 5GHz Sky Survey

First pulsar/ISM work

*M31 ATA-7*



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## First Science

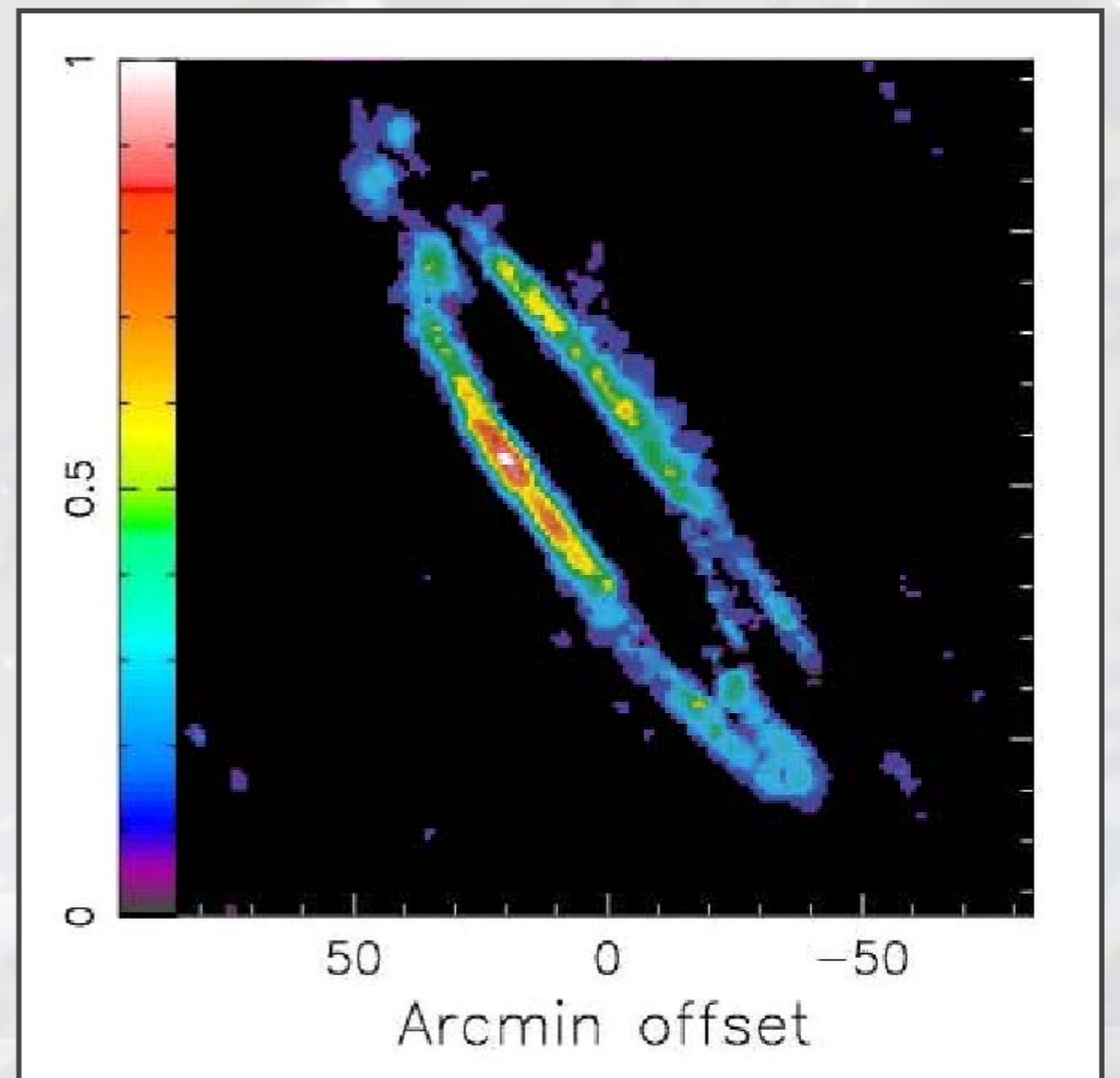
After July 1st, 2007

First SETI survey, 3 beams, 100MHz BW

FiGGS: 5GHz Sky Survey

First pulsar/ISM work

*M31 ATA-20*



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## Near future

Goals for 2nd half of 2007

Beamformer to 2 IFs, correlator to 42 elements

Goals for 2008

Double the size of array to 80 antennae

Upgrade FPGAs to Virtex 5, 4x faster each



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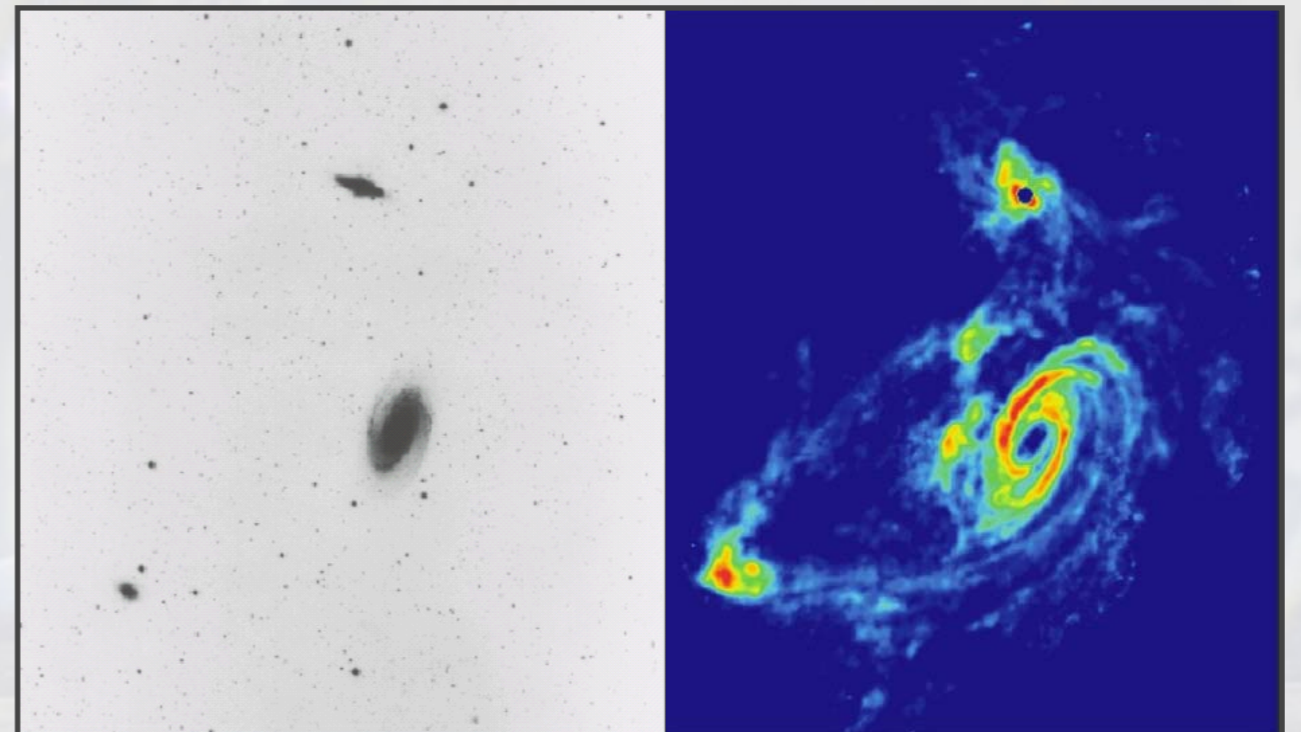
## Near-future science

Instantaneous multi-frequency timing  
Multi-frequency radio transient surveys  
(Pulsars, RRATs, bursters, orphan GRB  
afterglows)

Extend SETI/FiGGS survey area, sensitivity, and  
frequency

Extragalactic HI survey

*M81 Optical/HI*



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## Conclusions

ATA-42 first light before July 1st, 2007

Extremely versatile receivers and signal paths

Scalable back ends, continuously expanded

ATA-80 in 2008

Drives signal processing hardware development

ATA-350

Is 1% SKA

Is one impressive survey machine!



## Design Goals for the ATA

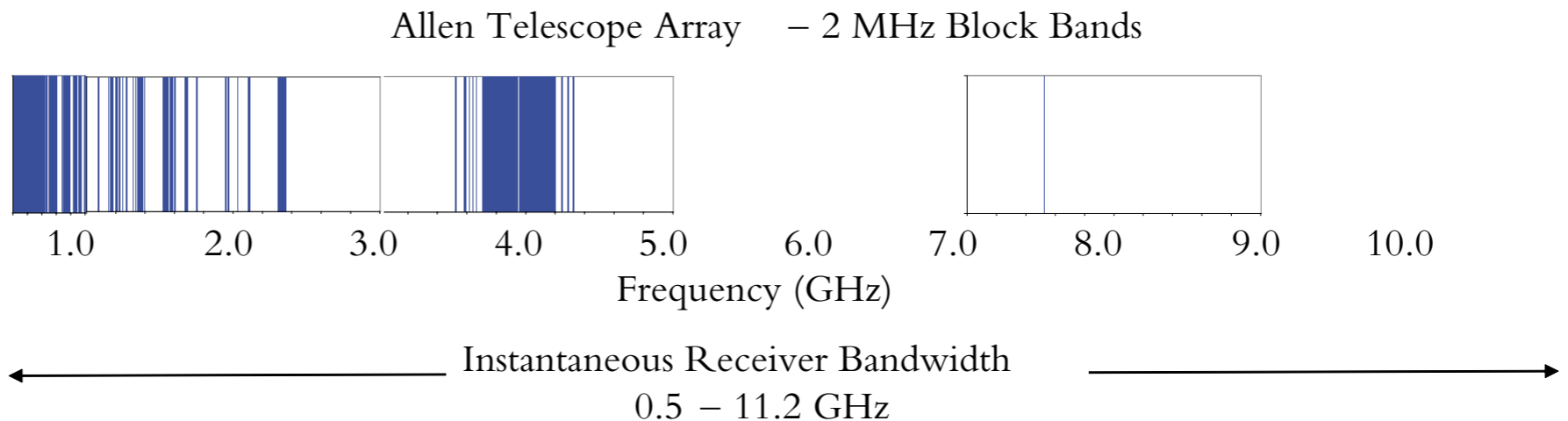
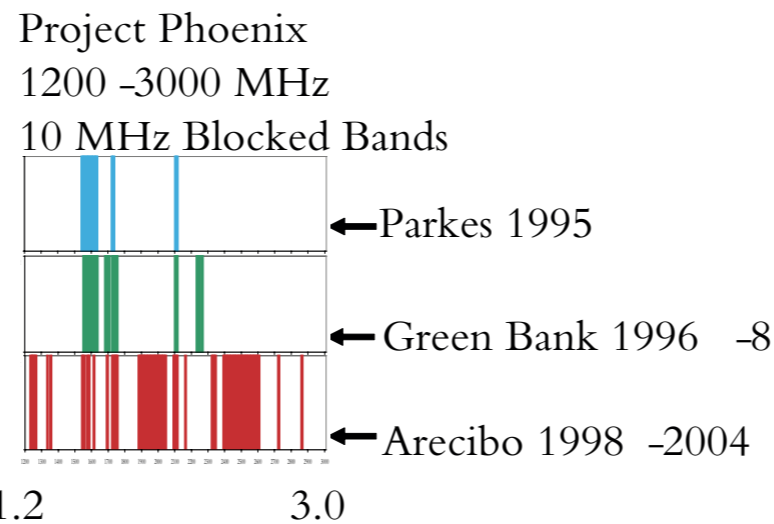
Number of elements	350		Site can hold more...
Element diameter	6.1	m	
Total geometric collecting area	10,229	m <sup>2</sup>	
	114	m	Diameter equivalent
Aperture efficiency	60	%	
System temperature	~42	K	At 60 K
$A_e/T_{\text{sys}}$	146	m <sup>2</sup> /K	~1% SKA
Effective diameter	700	m	Natural weighting
Number of tunings	4		Independent, concurrent
Number of beams	16		Dual -pol
Frequency	0.5	11.2	GHz
FoV	40	0.07	deg <sup>2</sup> (5 deg <sup>2</sup> at 1420 MHz)
Synthesized beam	216	10	arcsec



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## Interference Measurements at the Allen Telescope Array: Hat Creek Radio Observatory is quiet site.



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## BEE2 DSP Platform

The spectrometer is built on a Berkeley Wireless Research Center (BWRC) BEE2 (Berkeley Emulation Engine) platform. Originally designed for high-end reconfigurable computing applications such as DSP and ASIC oriented towards radio astronomy applications was developed as a collaboration between the BWRC, the UC Berkeley Radio Astronomy Lab, and the UC Berkeley SETI Group. The system consists of three main components: the main BEE2 processing board, a high-speed ADC board for data digitization, and an IBOB for high-speed serial communication between the two boards.

## BEE2 Board

The BEE2 board integrates high computational density with high-speed I/Os. Compute power is provided by its 5 Xilinx XC2VP70 Virtex-II Pro FPGAs (Field-Programmable Gate Array), each containing 328 18x18-bit multipliers, 2 PowerPC cores, 5904Kb of SRAM, and over 74,000 logic cells. In addition, each FPGA can be provided with up to 4GB of DDR2-SDRAM. External interfaces are available through 10Gb/s InfiniBand connections on the user FPGAs, as well as 100Mbps Ethernet and RS232 serial ports through the control FPGA.

## ADC Board

Analog data is digitized using an Atmel AT84AD001B dual 8-bit 1Gsample/s ADC. The ADC can be driven with either single-ended or differential inputs, and can digitize either 2 streams at 1Gsample/s or a single stream at 2Gsample/s. The board is designed to mate directly to an IBOB board for high-speed serial data I/O.

## IBOB Board

IBOB (InfiniBand BreakOut Board) boards allow a variety of I/O cards to provide data for packetization onto the InfiniBand protocol. Each board provides 2 Z-DOK+ connectors for I/O card attachment, and 2 CX4 InfiniBand connectors for interface to BEE2 boards. Data serialization is done by a Xilinx XC2VP50 FPGA. The FPGA provides 232 18x18-bit multipliers, 2 PowerPC cores, 4176Kb of SRAM in addition to 36Mbit of on-board ZBT SRAM, and over 53,000 logic cells, allowing the IBOB to pre-process data before handing off to the BEE2.

